CLAIMS

1. A field emission-type electron source including an insulative substrate and an electron source element formed on the side of one surface of said insulative substrate, said electron source element having:

a lower electrode;

a surface electrode; and

a strong-field drift layer including polycrystalline silicon and disposed between said lower electrode and said surface electrode, said strong-field drift layer allowing electrons to pass therethrough according to an electric field generated when a certain voltage is applied to said lower and surface electrodes in such a manner that said surface electrode has a higher potential than that of said lower electrode, said field emission-type electron source comprising:

a buffer layer provided between said strong-field drift layer and said lower layer, said buffer layer having an electrical resistance greater than that of said polycrystalline silicon.

2. The field emission-type electron source according to claim 1, wherein said buffer layer includes an amorphous layer.

3. The field emission-type electron source according to claim 1, in which a plural number of said electron source elements are formed on the side of said surface of said insulative substrate, wherein

said insulative substrate includes a glass substrate allowing infrared rays to transmit therethrough, and

said buffer layer includes a portion of a film which is made of a material capable of absorbing infrared rays and formed to cover the whole area on the side of said surface of said insulative substrate before the formation of said strong-field drift layer.

4. The field emission-type electron source according to claim 3, wherein said amorphous layer includes an amorphous silicon layer.

5. The field emission-type electron source according to claim 3, wherein said strong-field drift layer includes anodized porous polycrystalline silicon.

6. The field emission-type electron source according to claim 5, wherein said strong-field drift layer includes a plurality of columnar semiconductor crystals each formed along the thickness direction of said lower electrode, and

a number of nanometer-order semiconductor nanocrystals residing between said semiconductor crystals, each of said semiconductor nanocrystals having a surface formed with an insulating film which has a thickness less than the grain size of said semiconductor nanocrystal.

7. A method of producing the field emission-type electron source according to any one of claims 1 to 6, comprising:

forming the lower electrode on the side of said surface of said insulative substrate, and then forming the buffer layer on said lower electrode before forming the strong-field drift layer.

8. A method of producing the field emission-type electron source according to claim 6, comprising:

a lower-electrode forming step of forming the lower electrode on the side of said surface of said insulative substrate;

a first film-forming step of forming the buffer layer on the side of said surface of said insulative substrate after said lower-electrode forming step;

a second film-forming step of forming a polycrystalline semiconductor layer on the surface of said buffer layer;

a nanocrystallization step of nanocrystallizing at

least a portion of said polycrystalline semiconductor layer through an anodizing process to form the semiconductor nanocrystals; and

an insulating-film forming step of forming the insulating film on the surface of each of said semiconductor nanocrystals.

9. The method according to claim 8, wherein said second film-forming step is performed after said first film-forming step without exposing the surface of said buffer layer to the atmosphere.

10. The method according to claim 9, in which a plasma CVD process is used as a film-forming process in each of said first and second film-forming steps, wherein when said first film-forming step is shifted to said second film-forming step, a discharge power for said plasma CVD process is changed from a first condition for forming the buffer layer to a second condition for forming the polycrystalline semiconductor layer.

11. The method according to claim 9, in which a plasma CVD process is used as a film-forming process in each of said first and second film-forming steps, wherein when said first film-forming step is shifted to said second film-

forming step, a discharge pressure for said plasma CVD process is changed from a first condition for forming the buffer layer to a second condition for forming the polycrystalline semiconductor layer.

12. The method according to claim 9, in which a plasma CVD process or catalytic CVD process is used as a film-forming process in each of said first and second film-forming steps, wherein when said first film-forming step is shifted to said second film-forming step, the partial pressure ratio of source gases for said plasma CVD process or catalytic CVD process is changed from a first condition for forming the buffer layer to a second condition for forming the polycrystalline semiconductor layer.

13. The method according to claim 9, in which a plasma CVD process or catalytic CVD process is used as a film-forming process in each of said first and second film-forming steps, wherein when said first film-forming step is shifted to said second film-forming step, the kind of source gases for said plasma CVD process or catalytic CVD process is changed from a first condition for forming the buffer layer to a second condition for forming the polycrystalline semiconductor layer.

14. The method according to claim 8 or 9, which includes between said first and second film-forming steps a pre-growth treatment step of subjecting the surface of the buffer layer to a treatment for facilitating the creation of a crystal nucleus in the initial stage of said second film-forming step.

15. The method according to claim 14, wherein said pre-growth treatment step is a step of subjecting the surface of said buffer layer to a plasma treatment.

16. The method according to claim 14, in which said pre-growth treatment step is a step of subjecting the surface of said buffer layer to a hydrogen plasma treatment, wherein said second film-forming step includes forming a polycrystalline silicon layer serving as the polycrystalline semiconductor layer through a plasma CVD process using a source gas including at least a silane-based gas.

17. The method according to claim 14, wherein said pre-growth treatment step is a step of subjecting the surface of said buffer layer to an argon plasma treatment.

18. The method according to claim 14, wherein said pre-

growth treatment step is a step of forming a layer including a number of silicon nanocrystals, on the surface of said buffer layer.